Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A method of processing a wafer, comprising:

providing a wafer having initial thickness variations between two surfaces of said wafer;

processing said wafer through a first module, said first module comprising apparatus for performing a grinding process, a clean process and a metrology process, and said processing therethrough includes said grinding process, said clean process and said metrology process;

defining an edge profile on said wafer; and

processing said wafer through a second module, said second module comprising apparatus for performing a double side polish (DSP) process, a clean process and a metrology process, and said processing therethrough includes said DSP process, said clean process and said metrology process.

2. (Original) The method of claim 1 wherein said first module processing further comprises an etch process, said etch process reducing said wafer thickness by less than about ten (10) microns.

3. (Original) The method of claim 1 wherein said first module processing precedes said defining said edge profile.

4. (Original) The method of claim 1 wherein said first and second modules each comprise a cluster tool defining a clean room environment.

5. (Original) The method of claim 1 wherein said first module metrology process is simultaneous with said grinding process.

6. (Original) The method of claim 5 wherein said first module metrology process produces a metrology profile for said wafer, said processing through said first module further comprising modifying said grinding process in response to said metrology profile.

7. (Original) The method of claim 1 wherein said first module metrology process is after said grinding process.

8. (Original) The method of claim 1 further comprising polishing said edge of said wafer after said defining said edge profile.

9. (Original) The method of claim 1 further comprising processing said wafer through a third module, said third module comprising apparatus for performing a finish polish process, a clean process and a metrology process, and wherein said processing through said third module comprises said finish polishing process, said clean process and said metrology process.

10. (Original) The method of claim 9 further comprising, after completion of said processing through said third module, providing said wafer directly to a process chamber for fabrication of a semiconductor device.

11. (Original) The method of claim 9 further comprising, in order after completion of said processing through said third module, cleaning said wafer, inspecting said wafer, packaging said wafer, and delivering said wafer to a wafer process facility for subsequent fabrication of a semiconductor device.

12. (Original) The method of claim 1 wherein said wafer has a total thickness variation (TTV) between said two surfaces of less than about 0.3 microns after said processing through said second module.

13. (Original) The method of claim 1 wherein said wafer has a SFQR of less than 0.12 microns after said processing through said second module.

14. (Original) The method of claim 1 further comprising processing said wafer through at least a portion of said first module prior to processing a second wafer through said first module.

15. (Original) The method of claim 1 further comprising laser marking said wafer prior to said defining said edge profile.

16. (Original) The method of claim 1 further comprising performing a donor anneal process prior to said defining said edge profile.

17. (Original) The method of claim 1, further comprising processing said wafer through a third module, said third module comprising apparatus for performing said defining said edge profile, and an edge polishing process, said processing through said third module comprising said defining said edge profile and said polishing said wafer edge.

18. (Currently amended) A method of processing a wafer prior to device formation thereon, said method comprising, in order:

providing a wafer having first and second surfaces and a peripheral edge;

grinding said first and second wafer surfaces;

processing the peripheral edge, the processing comprising defining an edge profile of said wafer [[,]] and polishing said peripheral edge; and

polishing said first and second wafer surfaces.

Claims 19-25 (Canceled).

26. (New) The method as in claim 18 wherein defining the edge profile of the wafer comprises creating a beveled peripheral edge.

27. (New) The method as in claim 18 wherein defining the edge profile of the wafer comprises notching the wafer to create a primary flat portion of the peripheral edge.

28. (New) The method as in claim 18 wherein defining the edge profile of the wafer comprises notching the wafer to create a secondary flat portion of the peripheral edge.